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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,158	10/01/2003	Ming-Fang Wang	67,200-1160	8159

7590 05/18/2006

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EXAMINER	
GEORGE, PATRICIA ANN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,158	WANG ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11, and 13-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Amendment dated 02/28/06 is noted and filed. Claims 1, 6, 9, 13, 15, and 19 were amended to overcome prior art rejection; claims 10 and 12 were canceled; claims 21 and 22 are newly added.

Claim Objections

Claim 5 objected to because of the following informalities: The term "comprises a lowermost SiO2 layer formed over ... substrate" is confusing as it does not identify where the "high-k gate dielectric stack" of claim 1 is located. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 recites the limitations ""the gate dielectric layer stack comprises a lowermost SiO2 layer" in lines 1 and 2; and "over the silicon substrate". Since, claim 1 only refers to a high-k gate dielectric stack, what is the term "the stack" (which comprises a low-k material) referencing in claim 5? Again, claim 1 only references "a

substrate", thus, what is the term "the silicon" referencing? There is insufficient antecedent basis for both of these limitations in claim 5.

Claim 13 recites the limitation "about 10" in line 7. No unit terminology follows the number 10. There is insufficient antecedent basis for this limitation of claim 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 4, 6, 9, 13, 17, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Labelle et al. (2005/0101147) in view of Loan et al. (6,136,725).

As to claim 1, Labelle et al. teaches a method of treating a gate stack structure comprised of a gate electrode of polysilicon positioned over top of a high-k dielectric comprised of zirconium oxide, halfnium oxide and other high-k dielectric materials (para. 0003). Labelle et al.'s nitride treatment forms a barrier that can prevent undesirable lateral oxygen diffusion into the high-k dielectric segment during subsequent process

steps (i.e. reduce interface states between high-k dielectric and gate electrode) (see para. 0017). The plasma nitridation process is performed on the gate stack after the gate etch process (i.e. lithographically patterning and etching to form a gate structure) has been performed (see para 18).

Labelle et al. is silent as to the gate dielectric segment being a stack, as in applicants' limitation of claim 1.

Loan et al. teaches a method of forming extrememly thin films of different materials to make stacked gate dielectrics used to minimize gate capacitance, typically employed where increased device speed is needed (see col. 25, lines 35-43).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of plasma treating a gate stack, as in Labelle et al., by including that the high-k dielectric segment would consist of stacked gate dielectrics, as in Loan et al., because Loan teaches a variety of benifits, such as: minimize gate capacitance where increased device speed is needed (see col. 25, lines 35-43); deposition of sequential dielectrics in the same chamber which protects the wafer from being exposed to random oxidation which is destructive to the gate (see col. 25, lines 44-53); and because the wafer need not move the system would have intrinsically high throughput, known to reduce production time which is a cost saving for manufacturing (see col. 25, lines 44-53).

As to claim 2, Labelle et al. teaches a step of annealing after forming and treating the gate structure (para. 0016).

As to claims 4, 6, 9, 13, 17, 19, 21, and 22, see discussion toward claim 1 above.

Claim Rejections - 35 USC § 103

Claims 3, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Labelle et al. and Loan et al., as applied to claims 1-2, 4, 6, and 9 above, and further in view of Wolf (Silicon Processing for the VLSI Era, Volume 1; Process Technology; pg.58, para. 2, 1986 Latice Press; ISBN 0-9616721-3-7)

The modified teaching of Labelle et al. is silent as to the ambient annealing temperature of from about 600.degree. C. to about 750.degree. C., as in claim 3 and 14-15.

Wolf teaches a desirable option of Ar or N2 annealing (as in applicants' claim 15) that processing can be carried out extended from 420-1150 degree.C which encompasses applicants' range in claims 3 and 14.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of annealing after forming and treating the gate structure (para. 0016), as Labelle et al., by including the temperature range, as Wolf, because Wolf teaches it is known and a desirable option of annealing.

Claim Rejections - 35 USC § 103

Claims 5, 7, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Labelle et al. and Loan et al., as applied to claims 1-2, 4, 6, and 9 above, and further in view of Shinriki et al. (2005/0074983 CIP of PCT/JP03/03655).

Labelle et al. teaches away from a single layer of SiO.sub.2, however Labelle et al is silent as to the base dielectric layer of the gate stack comprising SiO.sub.2, as in claims 5.

Shinriki et al. teaches it is preferably to change the composition of the dielectric stack gradually from the SiO.sub.2 base to a composition primarily of high-k dielectric, as to avoid defects such as interface states (see para. 0006).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the teaching of a dielectric stack layer, as in Labelle, to include that the base comprise SiO.sub.2, as in Shinriki et al., because Shinriki et al. teaches it is preferable because it avoids defects such as interface states (see para. 0006).

As to claims 7, 16, and 18, see discussion above.

Claim Rejections - 35 USC § 103

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over the modified invention of Labelle et al., as applied to claims 5, 7, 16, and 18 above, and further in view of Sarigiannis et al. of 2004/0152304.

As to claim 8, the modified invention of Labelle is silent as to how the high-k dielectric materials may be formed, such as ALD (ALCVD) at less than 300 degree C, as in claim 8.

Sarigiannis et al.teaches an ALD deposition temperature of 200 degree C, (para.4, l.11), which is within the claimed range of less than about 300 degree C".

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a process temperature for ALD deposition, as Sarigiannis, when forming the gate structure, of Labelle, because Sarigiannis teaches it can be advantageous.

Claim Rejections - 35 USC § 103

Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Labelle et al. and Loan et al., as applied to claims 1-2, 4, 6, and 9 above, further in view of Steger (5,085,727).

As for claim 11, Labelle et al. teaches a plasma etcher may be used for the treatment process, however Labelle et al. is silent as to the pressure of the plasma treatment, as applicants' claim.

Steger teaches plasma etcher can operate in a range of between about 1 mTorr to about several Torr which is dependant on the type of plasma system used, (see col. 5, lines 31-39) and encompasses applicants' claimed range of about 100 mTorr to about 10 Torr.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of Labelle et al. to include the pressure ranges, as in Steger, because Steger teaches plasma etchers can be used at the specific pressures as applicants' limitations in claim 11 and 20, are known to be

effective. Since the reference of Steger does not limit the pressure range selected, one of ordinary skill would use a plasma etcher for the method of plasma treatment at any desired pressure, including applicants specifically claimed range.

Response to Arguments

Applicant's arguments filed 2/28/06 have been fully considered but they are not persuasive in view of the new grounds of rejection offered above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US 2003/0124824.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patricia A George
Examiner
Art Unit 1765

PAG
05/06

NADINE NORTON
SUPERVISORY PATENT
EXAMINER